

AMD Athlon™ 64 Processor Product Data Sheet



- **Compatible with Existing 32-Bit Code Base**
 - Including support for SSE, SSE2, SSE3*, MMX™, 3DNow!™ technology and legacy x86 instructions
 - *SSE3 supported by Rev E and later processors
 - Runs existing operating systems and drivers
 - Local APIC on-chip
- **AMD64 Technology**
 - AMD64 technology instruction set extensions
 - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
 - Eight additional 64-bit integer registers (16 total)
 - Eight additional 128-bit SSE registers (16 total)
- **Cache**
 - Two 64-bit operations per cycle, 3-cycle latency
- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
 - With advanced branch prediction
- **16-Way Associative ECC-Protected L2 Cache**
 - Exclusive cache architecture—storage in addition to L1 caches
 - 1 Mbyte, 512-Kbyte and 256-Kbyte options
- **Machine Check Architecture**
 - Includes hardware scrubbing of major ECC-protected arrays
- **Power Management**
 - Multiple low-power states
 - System Management Mode (SMM)
 - ACPI-compliant, including support for processor performance states

754-Pin Package Specific Features

- **Refer to the *AMD Functional Data Sheet, 754 Pin Package, order# 31410*, for functional, electrical, and mechanical details of 754-pin package processors.**
- **Electrical Interfaces**
 - HyperTransport™ technology: LVDS-like differential, unidirectional
 - DDR SDRAM: SSTL_2 per JEDEC specification
 - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications
- **Packaging**
 - 754-pin lidded micro PGA
 - 1.27-mm pin pitch
 - 29x29-row pin array
 - 40mm x 40mm organic substrate
 - Organic C4 die attach
- **Integrated Memory Controller**
 - Low-latency, high-bandwidth
 - 72-bit DDR SDRAM at 100, 133, 166, and 200 MHz
 - Supports up to three unbuffered DIMMs
 - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
 - One 16-bit link supporting speeds up to 800 MHz (1600 MT/s) or 3.2 Gigabytes/s in each direction

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939-Pin Package Specific Features

- Refer to the *AMD Functional Data Sheet, 939-Pin Package, order# 31411*, for functional, electrical, and mechanical details of 939-pin package processors.
- **Electrical Interfaces**
 - HyperTransport™ technology: LVDS-like differential, unidirectional
 - DDR SDRAM: SSTL_2 per JEDEC specification
 - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications
- **Packaging**
 - 939-pin lidded micro PGA
 - 1.27-mm pin pitch
 - 31x31-row pin array
 - 40mm x 40mm organic substrate
 - Organic C4 die attach
- **Integrated Memory Controller**
 - Low-latency, high-bandwidth
 - 144-bit DDR SDRAM at 100, 133, 166, and 200 MHz
 - Supports up to four unbuffered DIMMs
 - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
 - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction

Socket AM2 Specific Features

- Refer to the *Socket AM2 Processor Functional Data Sheet, order# 31117*, for functional and mechanical details of socket AM2 processors.
- Refer to the *AMD NPT 0Fh Family Processor Electrical Data Sheet, order# 31119*, for electrical details of socket AM2 processors.
- **Electrical Interfaces**
 - HyperTransport™ technology: LVDS-like differential, unidirectional
 - DDR2 SDRAM: SSTL_1.8 per JEDEC specification
 - Clock, reset, and test signals also use DDR2 SDRAM-like electrical specifications
- **Packaging**
 - Lidded micro PGA
 - 31x31 grid array
 - 1.27-mm pin pitch
 - Compliant with RoHS (EU Directive 2002/95/EC) with lead used only in small amounts in specifically exempted applications
- **Integrated Memory Controller**
 - Low-latency, high-bandwidth
 - 144-bit DDR2 SDRAM controller operating at up to 400 MHz
 - Supports up to four unbuffered DIMMs
 - ECC checking with double-bit detect and single-bit correct
- **HyperTransport™ Technology to I/O Devices**
 - One 16-bit link supporting speeds up to 1 GHz (2000 MT/s) or 4 Gigabytes/s in each direction

Revision History

Date	Revision	Description
September 2006	3.18	Public release. <ul style="list-style-type: none"> Added HyperTransport™ Technology information under Socket AM2 Specific Features. Removed change bars.
August 2006	3.16	Added RoHS compliance statement. Added asterisk note to SSE3.
June 2006	3.12	Public release. <ul style="list-style-type: none"> Clarified SSE3 support. Added Socket AM2 Specific Features Duplicated Electrical Interfaces under the 754-pin and 939-pin Specific Features.
April 2005	3.10	Added revision history. Removed multi core information.

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